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PRN No.	
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PAPER CODE	U213-232 (RE)
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December 2023 (REEXAM)

SY B.TECH (SEMESTER - I)

COURSE NAME: COMPUTER
ARCHITECTURE AND ENGINEERING
ORGANIZATION

BRANCH: COMPUTER
AND ENGINEERING

COURSE CODE:

CSUA21202

(PATTERN 2020)

Time: [2 Hrs]

[Max. Marks: 60]

Instructions to candidates:

- 1) Figures to the right indicate full marks.
- 2) Use of scientific calculator is allowed
- 3) Use suitable data wherever required
- 4) All questions are compulsory. Solve any two sub questions each from each Question 1, 2, 3, 4, 5, and 6 respectively

Q. No.	Question Description	Max. Marks	CO mapped	BT Level
Q.1	a) Discuss features of 8086 processor.	[5]	1	Understand
	b) Compare 8086 and 80386DX processor	[5]		
	c) Describe the Flag register of 80386 with diagram.	[5]		
Q2	a) Describe segment translation mechanism with diagram.	[5]	2	Understand
	b) Draw and explain Segment Selector.	[5]		
	c) Discuss the use of Granularity bit from Segment Descriptor.	[5]		
Q3.	a) Differentiate between CPL, DPL and RPL.	[5]	3	Analyze
	b) Explain page level protection in 80386DX.	[5]		
	c) Explain segment level protection using limit level checking.	[5]		

Q.4	<p>a) Explain memory hierarchy with diagram.</p> <p>b) Classify 2 types of cache addresses and explain it in detail with a diagram.</p> <p>c) Demonstrate the placing of cache memory in accordance with main memory with diagram.</p>	<p>[5]</p> <p>[5]</p> <p>[5]</p>	4	Apply
Q.5	<p>a) Solve division of the following numbers using restoring division algorithm:</p> <p>Dividend (A:Q) = 0000:0111 (7), Divisor (M)= 0011 (3)</p> <p>b) Draw and Explain flowchart Booth's algorithm with example.</p> <p>c) Explain IEEE standard for floating point Single precision format with diagram.</p>	<p>[5]</p> <p>[5]</p> <p>[5]</p>	5	Apply
Q.6)	<p>a) Illustrate the timing diagram for Instruction pipeline Operation.</p> <p>b) Sketch and explain the Internal structure of CPU.</p> <p>c) Draw and explain Data Flow Fetch Cycle .</p>	<p>[5]</p> <p>[5]</p> <p>[5]</p>	6	Apply