Total No. of Printed Pages: 2

PRN No.		PAPER CODE	U213-2105 (RE)

DECEMBER 2023 (~~ENSSEM~~ RE) EXAM

B. TECH (IT) (SEMESTER -I)

COURSE NAME: COMPUTER ORGANIZATION

COURSE CODE: ITUA21205

(PATTERN 2020)

Time: [2 Hrs] **[Max. Marks: 60]**

Instructions to candidates:

1) **Figures to the right indicate full marks.**
2) **Use of scientific calculator is allowed**
3) **Use suitable data wherever required**
4) **All questions are compulsory. Solve any two sub questions each from each Question 1 ,2, 3,4,5, and 6 respectively**

Q. No.	Question Description	Max. Marks	CO mapped	BT Level
Q.1	a) Interpret the structure and function *views* of computer.	[5]	1	3
	b) Suggest the techniques built into contemporary processors (Designing for performance of microprocessor speed).	[5]	1	3
	c) Calculate the data bus and address bus of following microprocessor's in terms of evolution of the Intel X86 architecture : 8080,8086,80286,80236,80486,Pentium, Pentium Pro, Pentium Pro, Pentium II, Pentium III, Pentium IV.	[5]	1	3
Q2	a) Apply the booth algorithm to multiply 25(multiplicand) by 13 (multiplier), where each number is represented by 6 bits.	[5]	2	3
	b) Apply the integer arithmetic to divide -119 by 11 in binary twos complement notation, using 12-bit words.	[5]		3
	c) Show the bit pattern for the following numbers in the floating point format : a) -720 and b) 0.645. Consider a floating point format with 8 bits for biased exponent and 23 bits for the significand.	[5]	2 2	3
Q3.	a) Explore and briefly define three types of superscalar instruction issue policies.	[5]	3	4
	b) Distinguish between hardwired and microprogrammed implementation of a control unit.	[5]	3	4
	c) Investigate the difference between instruction level parallelism and machine parallelism.	[5]	3	4
Q.4	a) Explore the addressing modes of 8086 microprocessor and explain any two.	[5]	4 4	4 4

	b) Analyze the instruction pipeline -pipeline strategy in 8086 microprocessors. c) Review the instruction format of 8086 microprocessor in terms of length, variable length instructions and pseudo code.	[5] [5]	4	4
Q.5	a) Contrast and explain the types of cache memory. b) Explore the elements of cache design. Explain any one in detail. c) Examine the operation of First In First Out algorithm in cache memory.	[5] [5] [5]	5 5 5	4 4 4
Q.6)	a) Distinguish between multicore and microprocessor architecture b) Contrast between single core and multi core architecture. c) Surmise the cache coherence problem in multi core architecture.	[5] [5] [5]	6 6 6	4 4 4

1: Remember 2: Understand 3: Apply 4: Analyze 5: Evaluate 6: Create