Total No. of Printed Pages: 02

PRN No.	

PAPER CODE	U213-2102(RE)

DECEMBER 2023 (REEXAM) EXAM

S.Y. (INFORMATION TECHNOLOGY) (SEMESTER - I)

COURSE NAME: DIGITAL ELECTRONICS AND MICROPROCESSOR

COURSE CODE: ITUA21202

(PATTERN 2020)

Time: [2 Hrs] **[Max. Marks: 60]**

Instructions to candidates:

1) **Figures to the right indicate full marks.**
2) **Use of scientific calculator is allowed**
3) **Use suitable data wherever required**
4) **All questions are compulsory. Solve any two sub questions each from each Question 1 ,2, 3,4,5,and 6 respectively**

Q. No.	Question Description	Max. Marks	CO mapped	BT Level
Q.1	a) i) Convert Hexadecimal (1BC) to Octal. ii) Convert Binary (10100011) to Decimal.	[5]	1	3
	b) Minimize the following expression using K-map method. F(A, B, C, D) = Σm(1, 3, 4, 6, 8, 9, 11, 13, 15) + Σd(0, 2, 14)	[5]	1	3
	c) i)Convert SOP to standard SOP F(A,B,C) = AB + AC' + BC ii)Convert POS to standard POS F(A,B,C) = (A+B).(A+C).(A+C')	[5]	1	3
Q2	a) Design the given expression using 8:1 multiplexer using LSB method F(A, B, C, D) = Σm (2,4,6,7,9,10,11,12,15)	[5]	2	3
	b) Design Half Adder and Half Subtractor using KMAP	[5]	2	3
	c) Design of BCD Adder using 4-bit Binary Adder	[5]	2	3
Q3.	a) Draw diagram of JK Flip flop and explain race around condition	[5]	3	3
	b) Convert J-K to D flip-flop. Represent the truth table, K-map simplification and circuit diagram.	[5]	3	3

	c) Demonstrate the working of SIPO and PISO shift registers.	[5]	3	2
Q.4	a) Design 3 bit Asynchronous up and down counter using JK-Flip Flops	[5]	4	3
	b) Design 3-bit Synchronous Down Counter using JK-Flip Flop	[5]	4	3
	c) Design Sequence generator 1-3-7-6 using JK-Flip Flops	[5]	4	3
Q.5	a) List and elaborate characteristics of digital ICs	[5]	5	4
	b) Draw and diseuss working of 2 input TTL NAND gate	[5]	5	3
	c) Draw and elaborate block diagram of PLA	[5]	5	3
Q.6)	a) Draw flag register of 8085 and discuss status of each flag with example	[5]	6	3
	b) Explain data transfer instructions with suitable examples.	[5]	6	2
	c) Elaborate Behavioral and Structural modelling styles used in VHDL with example.	[5]	6	2

Note: [BT Level – 1. Remember 2. Understand 3. Apply 4. Analyze 5. Evaluate 6. Create]