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DECEMBER 2023 (REEXAM)

S.Y. B.TECH. COMPUTER SCIENCE & ENGINEERING (AIML) (SEMESTER - I)

COURSE NAME: DIGITAL LOGIC AND COMPUTER ARCHITECTURE COURSE CODE: CMUA21204

(PATTERN 2020)

Time: [2 Hrs] **[Max. Marks: 60]**

Instructions to candidates:

1) **Figures to the right indicate full marks.**
2) **Use of scientific calculator is allowed**
3) **Use suitable data wherever required**
4) **All questions are compulsory. Solve any two sub questions each from each Question 1 ,2, 3,4,5,and 6 respectively**

Q. No.	Question Description	Max. Marks	CO mapped	BT Level
Q.1	a) Simplify following equation using appropriate technique f (A, B, C, D)= ∑m (2,7,8,10,11,13,15)	[5]	1	3
	b) Convert following equation into canonical SOP form Y= AB + $A\bar{C}$ +BC	[5]	1	3
	c) Minimize following equation using Quine McClusky Method f (A, B, C, D) = ∑m (0,2,3,6,7,8,10,12,13)	[5]	1	3
Q2	a) Implement following expression using 8:1 multiplexers f(A,B,C,D) = ∑m (0,2,3,6,8,9, 12, 14)	[5]	2	3
	b) Design full adder for two 1-bit binary numbers, show the truth table and logical diagram.	[5]	2	3
	c) Design combinational circuit for 1-bit magnitude comparator only for the following condition. "The first number is less than second number"	[5]	2	3
Q3.	a) Design serial in serial out left shift register for input 0110, show the working and timing diagram.	[5]	3	3
	b) Select appropriate register from following to multiply & divide 4 bit binary number by 2 and show the working of the same. i. Left Shift ii. Right Shift iii. Bidirectional Shift Register	[5]	3	3
			3	3

	c) Justify the need of M-S J-K flip flop and explain working of the same with diagram.	[5]		
Q.4	a) Design synchronous counter using appropriate flip flops for following sequence 4→6→7→3→1→4....	[5]	4	3
	b) Design 3 bit UP & Down Ripple Counter, show the working with timing diagram.	[5]	4	3
	c) Design sequence generator to generate following pulse train using shift registers 11001110	[5]	4	3
Q.5	a) A combinational circuit is defined by the function f1(A,B,C)= ∑m(4,5,7) and f2(A,B,C)= ∑m(3,5,7). Implement this circuit with PLA having 3 inputs, 3 product terms and 2 outputs.	[5]	5	3
	b) Implement 3 bit binary to gray converter using PLA i. Make a truth table ii. Simplify using K-Map iii. Realize using PLA iv. Specify the size of PLA	[5]	5	3
	c) Design an ASM chart and state diagram of 3 bit Down counter having one enable input such that E=1 Counting Enable E=0 Counting Disable	[5]	5	3
Q.6)	a) Justify the need of following addressing modes of 80386 microprocessor with example i. Register addressing Mode ii. Index addressing Mode iii. Based addressing Mode iv. Scaled Index addressing Mode v. Based Scaled Index addressing Mode	[5]	6	3
	b) Assume contents of accumulator and register C as 2EH and 6EH respectively, show the contents of the Accumulator, reg C, flag register bits Z, C, S, P and AC before and after execution of the instruction ADD C.	[5]	6	3
	c) Apply the instruction set of the 80836 microprocessor to write a assembly language program to display student name on the output screen using macro.	[5]	6	3

Note: [BT Level – 1. Remember 2. Understand 3. Apply 4. Analyze 5. Evaluate 6. Create