Total No. of Printed Pages: [2]

PRN No.	

PAPER CODE	U213-294 (RE)

December 2023 (RE-EXAM)

SY B.TECH (SEMESTER - I)

COURSE NAME: Digital System Design Branch: E&TC Engg. COURSE CODE: ETUA21204

(PATTERN 2020)

Time: [2Hr] **[Max. Marks: 60]**

(*) Instructions to candidates:

1) **Figures to the right indicate full marks.**
2) **Use of scientific calculator is allowed**
3) **Use suitable data wherever required**
4) **All questions are compulsory. Solve any two sub question from Question1 to Q6 each respectively**

Q. No.	Question Description	Max. Marks	CO mapped	BT Level
Q.1	**a)** Add and Subtract the following in binary. i) 1111 and 1010 ii)100100 and 10110	[5]	CO1	Apply
	b) Convert the following to the required form. i) $(101001.001)_2$= ( )$_{10}$ ii)$(A3B)_{16}$=( )$_{10}$	[5]	CO1	Apply
	c) Minimize the following expression using K-map and realize using NAND Gates, $F(A,B,C,D)=\sum m(0,1,2,9,11) + d(8,10,14,15)$.	[5]	CO1	Apply
Q.2	**a)** Simplify the Boolean function using K-Map $F(X,Y,Z)=\sum m(0,2,4,5,6)$ and draw the circuit diagram	[5]	CO2	Apply
	b) Design a three input majority function such that the output is 1 if the input has even number of 1's otherwise the output is 0.	[5]	CO2	Apply
	c) What is a Decoder? Construct a 4×16 decoder with two 3×8Decoders.	[5]	CO2	Apply
Q.3	**a)** What is meant by 'edge triggered'? Differentiate SR-FF and JK-FF with their functional operation and excitation tables.	[5]	CO3	Understand
	b) Convert a D-type flip-flop into T-flip-flop with the help of excitation table and K-map.	[5]	CO3	Apply
	c) Design and explain a 4-bit ring counter using D-flip flops with relevant timing diagrams	[5]	CO3	Apply
Q.4	**a)** i) Compare combinational and sequential circuits. ii) Explain about one bit binary cell.	[5]	CO4	Understand

	b) Design a mod-6 synchronous counter using D flip-flops.	[5]	CO4	Apply
	c) Design a Moore sequence detector to detect an overlapping sequence "101" using D flip-flops.	[5]	CO4	Apply
Q.5	**a)** Draw and explain the operation of 2 input TTL NOR gate	[5]	CO5	Understand
	b) CMOS logic family is superior than bipolar families," Justify	[5]	CO5	Understand
	c) Design CMOS circuit for $Y = \overline{(A+B).(C+D)}$	[5]	CO5	Apply
6	**a)** Write a VHDL code to design 1-bit full subtractor using dataflow modeling.	[5]	CO6	Apply
	b) Write a VHDL code for 4-bit up/down counter. If the up/down pin is 1 it should count in the Up mode and if 0 it should count in down mode	[5]	CO6	Apply
	c) Write a VHDL to implement a 2:1 multiplexer using structural style of model	[5]	CO6	Apply