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December 2023 (REEXAM)

SY B.TECH (SEMESTER - I)

COURSE NAME: MICROPROCESSORS Branch: AI & DS COURSE CODE:ADUA21203

(PATTERN 2020)

Time: [2 Hrs] **[Max. Marks: 60]**

(*) Instructions to candidates:

1) **Figures to the right indicate full marks.**
2) **Use of scientific calculator is allowed**
3) **Use suitable data wherever required**
4) **All questions are compulsory. Solve any two sub questions each from each Question 1, 2, 3, 4,5 and 6 respectively.**

Q. No.	Question Description	Max. Marks	CO mapped	BT Level
Q.1	a) How a computer system performs the "fetch" operation during the instruction cycle for following instruction: MOV A, 03 Which registers will be used during the operation? Explain with neat diagram.	[5]	[CO 1]	Understand
	b) How memory read operation is performed in 8086 microprocessor? Explain with one example.	[5]	[CO1]	Understand
	c) Consider a pipelined processor with the following four stages: IF : Instruction Fetch ID: Instruction Decode and Operand Fetch EX: Execute WB: Write Back The IF, ID and WB stages take one clock cycle each to complete the operation. The number of clock cycles for the EX stage depends on the instruction. The ADD and SUB instructions need 1 clock cycle and the MUL instruction needs 3 clock cycles in the EX stage. Operand forwarding is used in the pipelined processor. What is the number of clock cycles taken to complete the following sequence of instructions? ADD R2, R1, R0 : R2 ← R1 + R0 MUL R4, R3, R2 : R4 ← R3 * R2 SUB R6, R5, R4 : R6 ← R5 - R	[5]	[CO1]	ANALYZE

Q2	a) How does a three-level cache hierarchy improve the overall system performance compared to a single-level cache system? Illustrate with example and diagram.	[5]	[CO 2]	Understand
	b) Consider a direct mapped cache of size 16KB with block size of 256 bytes. The size of main memory is 128 KB. 1) Find number of bits in Tag. 2) Find the Tag Directory Size.	[5]	[CO2]	APPLY
	c) Explain the two primary cache write policies, namely Write-Through and Write-Back. Provide scenarios where each policy would be beneficial, and discuss the impact of these policies on the overall system.	[5]	[CO2]	ANALYZE
Q3.	a) Give the IEEE-754 floating point representation of 123.456 in single precision format	[5]	[CO 3]	APPLY
	b) How does the Booth's multiplication algorithm works when multiplying 12 by 4? Give step-by-step computations involved in obtaining the multiplication result.	[5]	[CO 3]	APPLY
	c)How does the Restoring Division Algorithm works when 11 is divided by 3? Give step by step computations involved in obtaining division result.	[5]	[CO3]	APPLY
Q.4	a) Identify the addressing mode in following instruction: MOV AX, [BX]+[DI] Calculate physical address when BX= 1000H, DI= 0010H and DS = 1000H Assume the content at physical address is 3412H. What will be contents of AH and AL register?	[5]	[CO 4]	APPLY
	b) Consider the following instructions: MOV AL, 1CH SAR AL, 1 RET What will be the contents of AL register and carry flag after execution of above instructions?	[5]	[CO 4]	APPLY
	c) Detail the flags register in the 80386DX processor. Highlight the purpose and impact of various flags on the execution of instructions.	[5]	[CO 4]	Understand
Q.5	a) Consider the Page reference string as: 7, 1, 0, 2, 0, 3, 0 ,4 ,2, 1, 0 with 4-page frame. Find the page fault ratio for given reference string using Optimal Page Replacement algorithm.	[5]	[CO 5]	APPLY
	b) Explain the significance of Translation Lookaside Buffer (TLB) in Paging mechanism.	[5]	[CO 5]	Understand

	c) How Global Descriptor Table Register (GDTR) is used to find Global Descriptor Table? Explain in detail with suitable diagram.	[5]	[CO 5]	Understand
Q.6)	a) Consider a scenario where a segment in an 80386 DX system has a privilege level set to 1. If an application running at privilege level 3 attempts to access this segment, determine whether this access will be allowed or denied according to the privilege level rules. Explain your reasoning.	[5]	[CO 5]	ANALYZE
	b) Discuss the role of privilege levels (Current Privilege Level, Descriptor Privilege Level, Requestor Privilege Level) in controlling access to both data and procedures within the 80386 DX protection mechanism.	[5]	[CO 5]	Understand
	c) How does limit checking contribute to memory access control and prevent unauthorized accesses? Provide an example illustrating the role of limit checking in ensuring secure memory operations.	[5]	[CO 5]	Understand