Total No. of Printed Pages; [2]

PRN No.	

PAPER CODE	U313-295-B-B3

December 2023 (ENDSEM) EXAM

TY B.TECH (SEMESTER - I)

COURSE NAME: System Design using Verilog Branch: E&TC COURSE CODE: ETUA31205B

(PATTERN 2020)

Time: [1Hr. 30 Min] **[Max. Marks: 40]**

(*) Instructions to candidates:

1) **Figures to the right indicate full marks.**
2) **Use of scientific calculator is allowed**
3) **Use suitable data wherever required**
4) **All questions are compulsory. Solve any one sub question from Question 3 and any two sub questions each from Questions 4, 5 and 6 respectively.**

Q. No.	Question Description	Max. Marks	CO mapped	BT Level
Q.1	What is the default size of Integer data type? What will be the size of Z deduced by the synthesis tool in the following example wire [15:0] X, Y; integer Z; Z = X + Y;	[2]	CO1	Understand

Q.2	Draw the logic diagram deduced the following Verilog code.
	module example (input a, b, c; output z)
	wire w1, w2;
	assign w1 = a^b;
	assign w2 = b & c;
	assign z = ~(w1 | w2);
	endmodule
		[2]	CO2	Understand

Q.3	**a)** Write a Verilog code to describe 4-input XOR gate using user defined primitives. **b)** Draw the circuit of 2-input CMOS NOR gate and write a Verilog code to design it using switch-level modelling.	[6] [6]	CO3 CO3	Apply Apply
Q.4	**a)** Compare FPGA with CPLD. **b)** Construct optimized square look-up table for decimal numbers 0 to 5 using ROM.	[5] [5]	CO4 CO4	Remember Apply

	c) Construct a circuit to implement following functions using PAL. Only three input OR plane is available. $F_1 = \sum m(0,1,2,4)$ *and* $F_2 = \sum m(0,5,6,7)$	[5]	CO4	Apply
Q.5	**a)** Construct an algorithm for GCD computation. Draw data path diagram with appropriate inputs/outputs and internal signals. Also draw ASM charts and state diagram. (Verilog code is not required)	[5]	CO5	Apply
	b) Design a sequence detector using Verilog to detect an overlapping sequence "1011" using Moore FSM. Draw state diagram. (Testbench is not required)	[5]	CO5	Apply
	c) Write a Verilog design code to design dual data port 2kB RAM with a word size of 8 bit. (Testbench is not required)	[5]	CO5	Apply
Q.6	**a)** List the micro-operations for the pipelined stage Memory Access (MEM). Also draw the stage diagram.	[5]	CO6	Understand
	b) Construct the pipelined architecture to do the following computations. Write a Verilog code to implement this architecture. x1 = A * B; x2 = C – D; x3 = x1 + x2; F = x3 / D;	[5]	CO6	Apply
	c) List the step-wise micro-instructions required to execute following instructions. i) LW R2, 200 (R6) ii) SW R3, 25 (R10)	[5]	CO6	Understand