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PRN No.	

PAPER CODE	U313-295 B (RE

December 2023 (REEXAM)

TY B.TECH (SEMESTER - I)

COURSE NAME: System Design using Verilog Branch: E&TC COURSE CODE: ETUA31205B

(PATTERN 2020)

Time: [2 Hrs] **[Max. Marks: 60]**

(*) Instructions to candidates:

1) **Figures to the right indicate full marks.**
2) **Use of scientific calculator is allowed**
3) **Use suitable data wherever required**
4) **All questions are compulsory. Solve any two sub questions each from each Question 1, 2, 3, 4, 5, and 6 respectively.**

Q. No.	Question Description	Max. Marks	CO mapped	BT Level
Q.1	**a)** Show VLSI Design flow and explain each step in the flow.	[5]	CO1	Understand
	b) Illustrate dataflow and behavioral style of modelling with the Verilog code example of each.	[5]	CO1	Understand

	c) What will be the value of outputs f1 and f2 if the input x = "10101010" and input y = "11110000" in the following code
	module example (input x, y, output f1, f2);
	wire [7:0] x, y; wire [4:0] f1; wire f2;
	assign f1 = x[4:0] & y[4:0];
	assign f2 = x[2] | ~y[3];
	endmodule
		[5]	CO1	Apply

Q.2	**a)** Realize 1-bit full adder using k-map and design it using Verilog.	[5]	CO2	Apply
	b) Realize 1-bit full subtractor using k-map and design it using Verilog.	[5]	CO2	Apply
	c) Write a Verilog module to generate the clock with a period of 10 ns. Use initial and always block.	[5]	CO2	Apply
Q.3	**a)** Write a Verilog module to implement 3-input NAND gate using user defined primitives.	[5]	CO3	Apply
	b) Write a Verilog module to implement negative edge triggered T-type flip-flop using user defined primitives.	[5]	CO3	Apply

	c) Draw the circuit diagram of CMOS 2:1 multiplexer. Write a Verilog module to implement it using switch-level modelling.	[5]	CO3	Apply
Q.4	**a)** Draw the architecture of XC9572 CPLD and explain each block.	[5]	CO4	Remember
	b) State important features and specifications of XC9500 CPLD family.	[5]	CO4	Remember
	c) State features of XC4000E FPGA family.	[5]	CO4	Remember
Q.5	**a)** Construct an algorithm for multiplication by repeated addition. Draw data path diagram with appropriate inputs/outputs and internal signals. Also draw ASM charts and state diagram. (Verilog code is not required)	[5]	CO5	Apply
	b) Design a sequence detector using Verilog to detect a nonoverlapping sequence "1011" using Moore FSM. Draw state diagram. (Testbench is not required)	[5]	CO5	Apply
	c) Write a Verilog design code to design 16 x 16 register bank with reset. (Testbench is not required)	[5]	CO5	Apply
Q.6	**a)** List the micro-operations for the pipelined stage Instruction Fetch (IF). Also draw the stage diagram.	[5]	CO6	Understand
	b) Construct the pipelined architecture to do the following computations. Write a Verilog code to implement this architecture. x1 = A * B; x2 = C + D; x3 = x1 - x2; F = x3 * C;	[5]	CO6	Apply
	c) List the step-wise micro-instructions required to execute following instructions. i) ADD R3, R6, R8 ii) SW R2, 30 (R10)	[5]	CO6	Understand