Total No. of Questions – [3] Total No. of Printed Pages: 2

G.R. No.	

PAPER CODE	U212-244 (ESE-DSY)

JULY 2023 (ENDSEM) EXAM

S.Y (E&TC) DSY (AY 2022-23 SEMESTER - I)

COURSE NAME: Digital System Design

COURSE CODE: ETUA21204

(PATTERN 2020)

Time: [1Hr] [Max. Marks: 30]

(*) Instructions to candidates:

1) **Use of scientific calculator is allowed**
2) **Use suitable data where ever required**
3) **All questions are compulsory**

Question No.	Question Description	Marks	CO mapped	Blooms Taxonomy Level
Q.1 a	Show how an asynchronous counter with D flip-flops can be implemented having a modulus of thirteen with a straight binary sequence from 0000 through 1100. Draw the timing diagram for the same	4	CO4	Applying
Q.1 b	Design a Mealy state machine for detecting a sequence bit stream of 110.	6	CO4	Applying
	OR			
Q1 c	Design a counter to produce the following binary sequence 1, 4, 3, 5, 7, 6, 2, 1. Use J-K flip-flops.	6	CO4	Applying
Q.2 a	CMOS logic family is superior than bipolar families," Justify	4	CO5	Understand

Q.2 b	Design 2 input TTL NAND gate and verify the truth table of it from your design.	6	CO5	Applying
	OR			
Q.2 c	Using PLA realize the follow expressions: F_1 (A, B, C) = $\sum$m (0, 3, 4, 7) and F_2 (A, B, C) = $\sum$m (0, 2, 4) Optimize expressions using k-map before implementation.	6	CO5	Applying
Q.3 a	Elaborate different Modeling styles used in VHDL.	4	CO6	Understand
Q.3b	Elaborate test bench for 3 bit ALU design.	6	CO6	Applying
	OR			
Q.3c	Design 2:1 multiplexer using any style of modelling	6	CO6	Applying