Total No. of Questions – [3] Total No. of Printed Pages: 02

G.R. No.	

PAPER CODE	223-243 (BSE)

May 2023 (ENDSEM) EXAM

S.Y. (E&TC) (AY 2022-23 SEMESTER - II)

COURSE NAME: Analog Circuits

COURSE CODE: ETUA22203

(PATTERN 2020)

Duration: [1 Hr] [Max. Marks: 30]

(*) Instructions to candidates:

1) **Use of scientific calculator is allowed**
2) **Use suitable data where ever required**
3) **All questions are compulsory**

Question No.	Question Description	Max. Marks	CO mapped	BT Level
Q.1	a) Describe with the help of circuit diagram and frequency response how opamp can be used to pass all the signals with frequencies greater than cut off frequency.	[4]	[CO4]	[Apply]
	b) Design the second order Butterworth low pass filter for cut off frequency 1 kHz. Use the capacitor of 0.1 micro farad. What will be the gain of the filter at the frequency 100 Hz? Comment on the roll off rate. (Note: Design should be supported with the circuit diagram)	[6]	[CO4]	[Apply]
	OR			
	c)With the circuit diagram and the frequency response, explain how the order of filter affects the frequency response of the filter? What will be the roll off rate of HPF if the order of the filter is made 4?	[6]	[CO4]	[Apply]
Q.2	a) Define resolution of the DAC. Find the no. of bits of the DAC if the output voltage is desired to change in 0.1 mV increments while using a reference voltage of 8 V.	[4]	[CO5]	[Apply]

	b) Justify R-2R ladder DAC is better than binary weighted DAC. A 3-bit binary weighted DAC has a reference voltage of 5 V. If R_f = 10 KΩ and R = 2 KΩ find equivalent analog output voltage for inputs 011 and 110.	**[6]**	[CO5]	[Analyze].
	OR			
	c) List advantages and disadvantages of Flash ADC. A 10-bit ADC accepts an input signal within a range of 0 to 12 V. (1) What is the minimum value of input voltage required to generate a change of 1LSB at the output? (2) What should be the input voltage to get all 1s at the output? (3) What will be the digital output for an input voltage of 6V?	**[6]**	[CO5]	[Apply]
Q.3	a)In PLL IC 565 determine free running frequency, lock range and capture range. Given demodulation capacitor C= 1 micro Farad, Resistor and capacitor of VCO, R1= 15 k ohms and C1= 0.01 micro farad. Vcc= 12 V and –Vcc=0 V (gnd)	**[4]**	[CO6]	[Apply]
	b) Describe how PLL is used as frequency multiplier and frequency demodulator?	**[6]**	[CO6]	[Understand]
	OR			
	c) i)Describe the working of PLL wrt the block diagram ii) Draw the transfer characteristics of PLL and describe its working with its different modes of operation.	**[6]**	[CO6]	[Understand]