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PRN No.	

PAPER CODE	U124-395

May 2024 (ENDSEM) EXAM

F.Y.B. TECH. (SEMESTER - II)

COURSE NAME: Digital Electronics **Branch: E&TC** **COURSE CODE:** ET12235

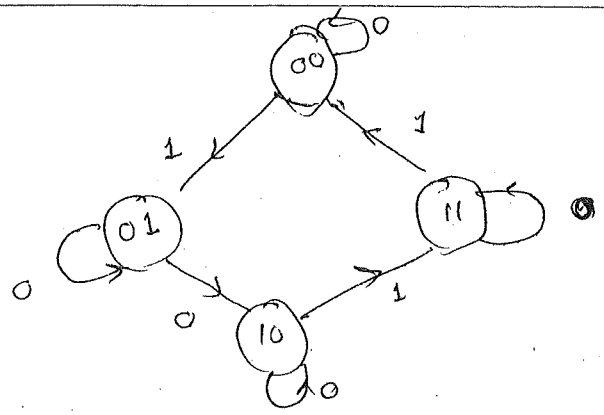
(PATTERN 2023)

Time: [1Hr. 30 Min] **[Max. Marks: 40]**

(*) Instructions to candidates:

1) **Figures to the right indicate full marks.**
2) **Use of scientific calculator is allowed**
3) **Use suitable data wherever required**
4) **All questions are compulsory. Solve any one sub question from each Question 1 and 2 and any three sub questions each from Questions 3 and 4.**

Q. No.	Question Description	Max. Marks	CO mapped	BT Level
Q.1	a) i. Convert the given Gray code number to equivalent binary 001001011110010	[5]	CO1	Understand
	ii. Consider a function 'F'. Show that F.F'=0 and F+F'=1	[5]		
	b) Minimize the following function using K-map F(P, Q, R, S) = Σm (4, 5, 6, 7, 8, 12) + d (1, 2, 3, 9, 11, 14)		CO1	Understand
Q2	a) Design a combinational circuit with the three inputs and one output. the output is equal to logic-1 when the binary value of the input is less than 4 otherwise the output is logic-0	[5]	CO2	Apply
	b) Implement the given logic function using a 4 : 1 multiplexer. f (A,B,C) = ∑m (0, 2, 4, 6).	[5]	CO2	Apply
Q.3	a) Convert D flip flop into JK flip flop.	[5]	CO3	Apply
	b) Design and implement 3-bit synchronous counter using T flip flop.	[5]	CO3	Apply
	c) Design the sequential circuit for the given state diagram using T flip flop.	[5]	CO3	Apply

	 d) Design and implement circuit using D flip flop to detect the binary sequence 110.	[5]	CO3	Analyze
Q.4	**a)** Elaborate different Modeling styles used in VHDL.	[5]	CO4	Understand
	b) Write a VHDL code to design 1-bit full subtractor using dataflow modeling.	[5]	CO4	Apply
	c) Write a VHDL to implement a 2:1 multiplexer using structural style of model	[5]	CO4	Apply
	d) Design a 3 bit ALU which can perform any 4 logical operations and 4 arithmetic operations.	[5]	CO4	Apply